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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,133	01/23/2001	Ritsuko Nagao	SEL 236	3327

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EXAMINER
PHAM, THANH V

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No.	Applicant(s)	
	09/768,133	NAGAO ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30-91, 93-101, 103-111, 113-184* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30-91, 93-101, 103-111, 113-184* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30-91, 93-101, 103-111, 113-184 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in combination with Chen U.S. Patent No. 5,453,406, Tang et al. US 5,550,066 and Hanihara et al. US 5,990,988.

The applicant's admitted prior art for the TFT formation to form a display device having pixel electrodes and an insulative layer over the pixel electrodes is similar to the instant invention, having use of an organic material where a low dielectric property is considered (the instant specification, pages 1-2 and 7).

> An active matrix liquid crystal display device is widely used for OA equipment, television sets and the like.
>
> The substrate is spun so that the varnish is uniformly applied thereto. The substrate on which the varnish is applied is baked in an oven or on a hot plate to obtain an insulating film.
>
> The thickness of the insulating film is controlled by the number of spinnings, the period of spinning time, the concentration and the viscosity of the varnish. A material used for spin-coating can be selected from a polyimide resin, an acrylic resin, a resin containing a siloxane structure, an inorganic SOG (Spin on Glass) material and the like, in consideration of physical properties such as a transparence, a heat resistance, a chemical resistance, and a thermal expansion coefficient. In the case where a low dielectric property is considered as an important factor, an organic material is often used.
>
> FIG. 2 shows a cross section of a conventional active matrix substrate. On a glass substrate 100, level differences generated by an active layer (including a

channel region 101, a source region 102, and a drain region 103), a gate wiring 105, a source wiring 107, a drain wiring 108 and the like are present. A leveling resin, representatively an acrylic resin, is used to as a first leveling film 109 so as to level these level differences. Finally, a pixel electrode 111 is formed on the first leveling film 109 to complete the active matrix substrate.

Next, as shown in FIG. 3, the active matrix substrate is bonded to a counter substrate 120 so as to interpose liquid crystal 123 therebetween to form a liquid crystal display device. According to this conventional method of forming a leveling film, however, it is apprehended that the pixel electrode 111 might be broken because of insufficient flatness of the leveling film. Moreover, since the unevenness due to the level differences remains on the surface of the pixel electrode 111, poor orientation of the liquid crystal 123 is caused on the uneven region of the surface.

As being seen in fig. 2, the wiring is connected to the semiconductor film through a first hole in the interlayer insulating film on the interlayer insulating film and the pixel electrode is connected to the wiring through a second hole. In applicant's admitted prior art fig.3, an electro luminescence layer 112 is formed over the pixel electrode 111.

In the Summary of the Invention, the instant specification states, "a TFT is formed in a similar manner as in the prior art shown in Fig. 2".

The applicant's admitted prior art lacks the second leveling layer over the first leveling layer.

The Chen reference discloses a method for producing a planar surface (col. 2, lines 64-67) wherein the thickness of a first leveling film 40 (2,000-3,000 Angstroms, col. 6, lines 1-10) formed above a wiring 34 is thinner than that of a second leveling film 42 (4,000-6,000 Angstroms, col. 6, line 53-54) formed on the first leveling film. Both first

and second leveling films are formed by spin coating and by the same material (col. 6, line 30). The method could be used to coat a display device.

In Chen's fig. 7, a second spin-on-glass layer 42 is formed over the first spin-on-glass layer 40 essentially planarizing the dielectric layer and completing the process. This second spin-on-glass layer 42 is formed by also using the liquid precursor of the siloxane type similar in composition to the material used for the first spin-on-glass layer 40, but in this second coating the spin-on-glass is dispensed at a significantly higher spin speed and at a constant speed. The same series of spin-on-glass is used for both layers.

The Chen reference further discloses, col. 5, lines 24-29

> insulating layer 32 is deposited thereon (on devices' conducting layers) by conventional means. For example, the insulating layer can be composed of silicon dioxide and silicon nitride and deposited using CVD or LPCVD.

and col. 6, line 67 to col. 7, line 15

> Although this embodiment describes a process for forming a single planar dielectric layer over a single patterned conducting layer, it should also be well understood by one skilled in the art that the process can be repeated to form additional patterned metal layers having planarized dielectric layer formed thereon. This can be accomplished by first depositing a second insulating barrier layer over the cured second spin-on-glass layer 42, forming via hole openings in the planar dielectric layer to the underlying conducting layer and then depositing a second conducting layer, such as aluminum, which contacts the first conducting layer through the via holes, the conducting layer can then be patterned by reactive ion etching and then planarizing process ARIC SOG of this invention can be used to planarize the second level metal. By repeating this process by the above method a multilayered metallurgy can be fabricated.
>
> The passivating layer of an insulating material *such as silicon oxide (Tang et al., col. 7, line 30), silicon nitride or silicon oxide (Chen, col. 5, lines 24-27) as same as "Specific insulators include noncrystalline compounds such as silicon oxide, silicon*

nitride, or silicon nitride oxide," *Nishimura et al. US 6,332,835, col. 7, lines 64-6 and/or "the insulating film formed on the data line, not only an oxide film, but also a nitride film or oxide-nitride film may be used", Tsuji et al. US 5,821,622, col. 27, lines 2-4,* is well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the applicant's admitted prior art with the second leveling layer as taught by Chen because the second leveling layer of Chen would provide the prior art structure with planarity over the formed TFT to prevent the pixel electrode from rough topography and improve the optical resolution (Chen's col. 1, lines 18 and 29). *With this combination, the pixel electrode would be connected to the wiring through a second hole formed in the passivating/insulating film (of silicon nitride, silicon oxide nitride or silicon oxide as well-known in the art) and the leveling film on the wiring as claimed.*

Choice of thickness of the leveling layers would depend on many other factors such as the gap between the protruded elements or the height of the protruded element and would be obtained by routine experimentation, MPEP 2144.05. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the appropriate thickness such as the thickness in the ranges as claimed into the process as the thickness would be selected in accordance with the surface planarity formation as taught by Chen.

Re claim 8, the applicant's admitted prior art discloses the driving TFT section but not the section of pixel TFT for controlling electric current to the EL element therefore it

does not show the EL cathode. However, the formation of a cathode made of a conductive film having a light shielding property is known in the art as EL cathode 84 in the Tang et al.'s figs. 3 and 9 and the associated passages. The Tang et al. reference also teaches "*a passivating layer 74 of an insulating material*, preferably silicon dioxide, is deposited over the surface of the device (the wiring 62/72)", col. 7, lines 30-35.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with the formation of a cathode made of a conductive film having a light shielding property of Tang et al. because the formation of a cathode made of a conductive film having a light shielding property of Tang et al. would provide the method of the combination with sufficiently low temperature fabrication (abstract and col. 2, line 61, e.g.)

The applicant's admitted prior art does not disclose the wiring is a three-layered laminated film containing a first titanium, an aluminum film and a second titanium film. The Hanihara et al. reference teaches "the wiring layers 31, 32,33 and the pixel electrode layer 34 are films made of such conductive metals as ... layers of titanium and aluminum formed by sputtering or evaporation or photolithography" (col. 6, lines 18-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with the layers of titanium and aluminum as taught by Hanihara et al. because the layers of titanium and aluminum for the wiring would provide the device formed by the combination with controllability (col. 1, line 9).

Response to Arguments

3. Applicant's arguments filed 11/10/2005 have been fully considered but they are not persuasive. Applicants only state that those claimed features are not disclosed or suggested by the cited references after providing some reasons to the change in the amended claims without any argument to the previous rejection.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-186. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TwP
11/21/2005

George Fourson
Primary Examiner